21 ~~23~~. (New) A variable gain circuit comprising:

a first variable gain amplifier which receives an input signal, outputs an amplified signal, and includes a first field-effect transistor;

a first gain control signal compensation circuit which outputs a first gain control signal for controlling a gain of the first variable gain amplifier and includes a second field-effect transistor; and

a gain deviation correction circuit including a second variable gain amplifier connected to an output of the first variable gain amplifier, and a second gain control signal compensation circuit which outputs a second gain control signal for controlling a gain of the second variable gain amplifier to correct a gain deviation based on the first variable gain amplifier.

REMARKS

Favorable reconsideration of this application is respectfully requested.

The specification has been amended to correct two minor typographical errors.

Claims 1-23 are now present in this application, claims 21-23 being added by way of the present amendment. Each of claims 21-23 is believed to be clearly supported by the specification, and thus no question of introduction of new matter is believed to be raised.

A separate letter to the Official Draftsperson has been sent to label Figures 16, 17A and 18 as prior art, and to correct minor informalities noted in Figures 3 ,14 and 15. No new matter has been added.

Claims 1 and 2 stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,172,567 (Ueno et al). Claims 3-14 were found to be allowable if rewritten in independent form and claims 15-20 have been allowed.

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The Applicants gratefully appreciate the allowance of claims 15-20 and the finding of claims 3-14 to recite patentable subject matter. Claims 3 and 9 have been rewritten in independent form, including the elements of claim 1, and have been further amended to make some minor grammatical changes. Accordingly, claims 3-14 are in condition for allowance.

In the present invention as recited in claim 1, a variable gain circuit includes a gain control signal compensation circuit for controlling a gain of a variable gain amplifier, and a gain deviation circuit connected to the variable gain amplifier which corrects a gain deviation based upon the variable gain amplifier and the gain control signal compensation circuit. In one non-limiting example, a variable gain amplifier 101 is gain controlled by a gain control signal generated by the gain control signal compensation circuit 102. The gain deviation inherent to the variable gain amplifier and the gain control signal compensation circuit is corrected by the gain deviation correction circuit. In this non-limiting example, the gain deviation occurs when $I_{D1}=I_{D2}$, $I_{D1}=I_0\text{-}\exp(-b\cdot V_x)$ and $I_{D2}=I_0-I_{D1}$, where I_0 is a constant current, b is a constant and V_x is an internal gain control signal. The variable gain control circuit can exhibit a linear gain characteristic.

Turning to the §102(e) rejection, Ueno et al disclose a radio-frequency power amplifier, wherein gate voltages Vg1, Vg2 and Vg3 of first, second and third FETs are controlled through a power control terminal Vapc. A correction circuit 40 is provided between the power control terminal Vapc and the third FET (column 7, lines 3-9). In other words, correction circuit 40 is provided for correcting a final stage amplifier including the third FET.

In comparing the circuit of Ueno et al to claims 1 and 2, FET Q1 was found to correspond to the recited first FET, FET Q3 was found to correspond to the recited second FET, and FET Q2 was found to correspond to the recited gain deviation correction circuit. The signal produced by the FETs Q2 and Q3 is supplied to FET Q1 for gain compensation. In claim 1, the gain control signal produced by the gain control signal compensation circuit

including the second FET is output to the variable gain amplifier having the first FET to control the gain thereof. The gain deviation of the variable gain amplifier is corrected by the gain deviation correction circuit based upon the variable gain amplifier and the gain control signal compensation circuit. The gain deviation circuit is connected to the amplifier and corrects a gain based upon the amplifier and the gain control circuit. There is no suggestion or disclosure in Ueno et al of a gain control compensation circuit and a gain control deviation correction circuit as recited in claim 1. Ueno et al does not describe how Q3 is connected to Q1 and corrects a gain deviation based upon Q1 and Q2. Accordingly, claims 1 and 2 are not anticipated by Ueno et al and withdrawal of the 35 U.S.C. § 102(e) rejection is respectfully requested.

It is respectfully submitted that the present application is in condition for allowance and a favorable decision to that effect is respectfully requested.

Respectfully submitted,

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Amendment Filed: September 17, 2002

IN THE SPECIFICATION

Page 14, beginning at line 8, please replace the paragraph as follows:

--The second operation is performed to correct the gain deviation due to the transition of the operation region of each MOSFET from a strong inversion region to a weak inversion region. FIG. 1C is a graph showing this [correct] correction. Note that the second correction is not required when FETs having no inverted layers, e.g., J-FETs (Junction Field-Effect Transistors) or MESFETs(Schottky junction field effect transistors), are used. By performing the corrections shown in FIGS. 1B and 1C, a linear-in-dB characteristic can be obtained even if MOSFETs are used. FIG. 1D shows this characteristic.--

Page 18, beginning at line 13, please replace the paragraph as follows:

--A transistor M1 has drain and gate terminals connected to each other. I_{D1} is input to the drain terminal. The drain terminal of a transistor M2 is connected to a power supply voltage V_{DD}, and its source terminal is connected to the source terminal of the transistor M1 and grounded via a current source Io. [a] A given power supply V_{BB} is connected to the gate terminal of the transistor M2. The current I_{D2} flowing in the drain terminal of the transistor M2 is the difference current between the current from the current source Io and the current I_{D1} (I_{D2} - Io - I_{D1}). Referring to FIG. 4, the drain terminal of the transistor M2 is connected to the power supply voltage V_{DD}. However, no problem arises even if the connection of the drain terminal changes as long as a current flows to satisfy I_{D2} = Io - I_{D1}.--

IN THE CLAIMS

--1. (Amended) A variable gain circuit comprising:

a variable gain amplifier which receives an input signal, outputs an amplified signal, and includes a first field-effect transistor;

a gain control signal compensation circuit which outputs a gain control signal for controlling a gain of said variable gain amplifier and includes a second field-effect transistor; and

a gain deviation correction circuit which is connected to the variable gain amplifier and corrects a gain deviation based on said variable gain amplifier and said gain control signal compensation circuit.

3. (Amended) [The circuit according to claim 1, which further comprises] A variable gain circuit comprising:

a variable gain amplifier which receives an input signal, outputs an amplified signal, and includes a first field-effect transistor;

a gain control signal compensation circuit which outputs a gain control signal for controlling a gain of said variable gain amplifier and includes a second field-effect transistor;

a gain deviation correction circuit which corrects a gain deviation based on said variable gain amplifier and said gain control signal compensation circuit; and

a gain control signal converter which converts an external gain control signal into an internal gain control signal, said variable gain amplifier including the first field-effect transistor [is] being a first variable gain amplifier, the first gain control signal [is] being a first gain control signal, said gain control signal compensation circuit including the second field-effect transistor [is] being a first gain control signal compensation circuit,

said gain deviation correction circuit [includes] including a second gain control signal compensation circuit and a second variable gain amplifier, [and]

said first gain control signal compensation circuit [converts] converting the internal gain control signal into the first gain control signal and [inputs] inputting the first gain control signal to said first variable gain amplifier to control gain of said first variable gain amplifier, and

said second gain control signal compensation circuit [converts] converting the internal gain control signal into the second gain control signal and inputs the second gain control signal to said second variable gain amplifier to control gain of said second variable gain amplifier.

9. (Amended) [The circuit according to claim 1, which further comprises] A variable gain circuit comprising:

a variable gain amplifier which receives an input signal, outputs an amplified signal, and includes a first field-effect transistor;

a gain control signal compensation circuit which outputs a gain control signal for controlling a gain of said variable gain amplifier and includes a second field-effect transistor;

a gain deviation correction circuit corrects a gain deviation based on said variable gain amplifier and said gain control signal compensation circuit;

a gain control signal converter which converts an external gain control signal into an internal gain control signal, said variable gain amplifier including the first field-effect transistor [is] being a first variable gain amplifier, said gain control signal compensation circuit including the second field-effect transistor [is] being a first gain control signal compensation circuit,

said gain deviation correction circuit [includes] including a second gain control signal compensation circuit and a second variable gain amplifier,

said first gain control signal compensation circuit [converts] converting the internal gain control signal into a first gain control signal,

said second gain control signal compensation circuit [converts] converting the first gain control signal into a second gain control signal, and the first gain control signal [is] being input to said first variable gain amplifier to control a gain of said first variable gain amplifier, and the second gain control signal [is] being input to said second variable gain amplifier to control a gain of said second variable gain amplifier.

Claims 21-23 (New).--

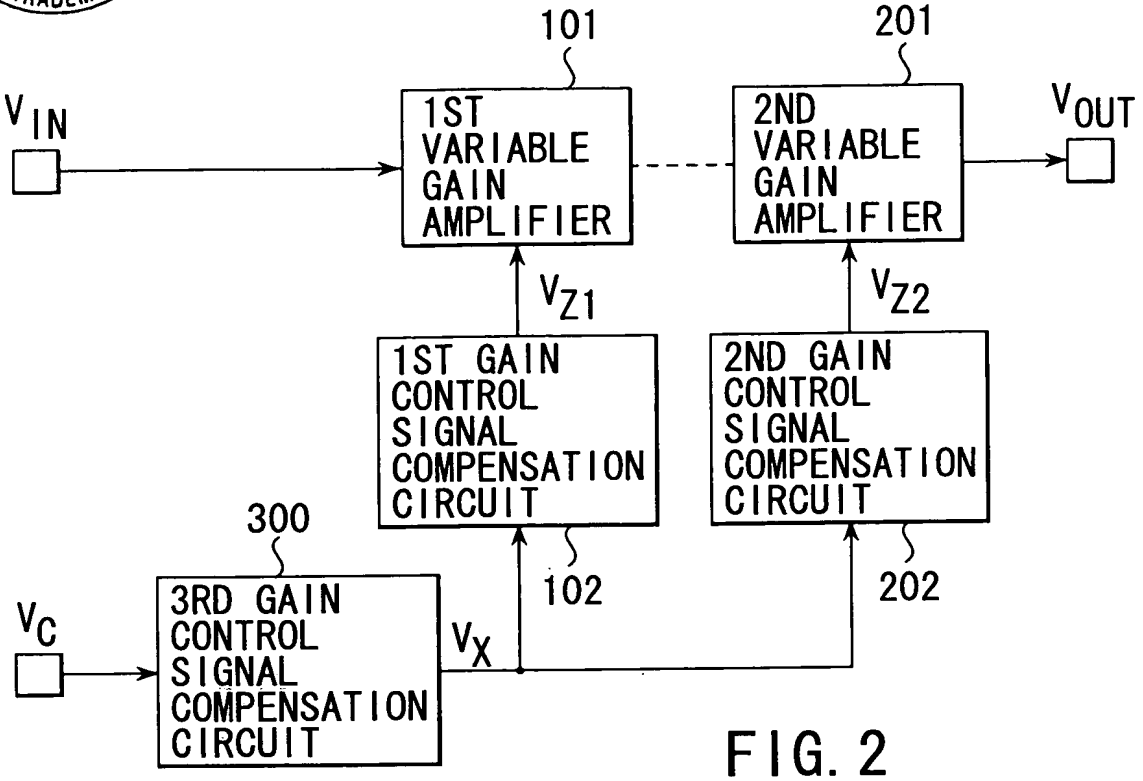

FIG. 2

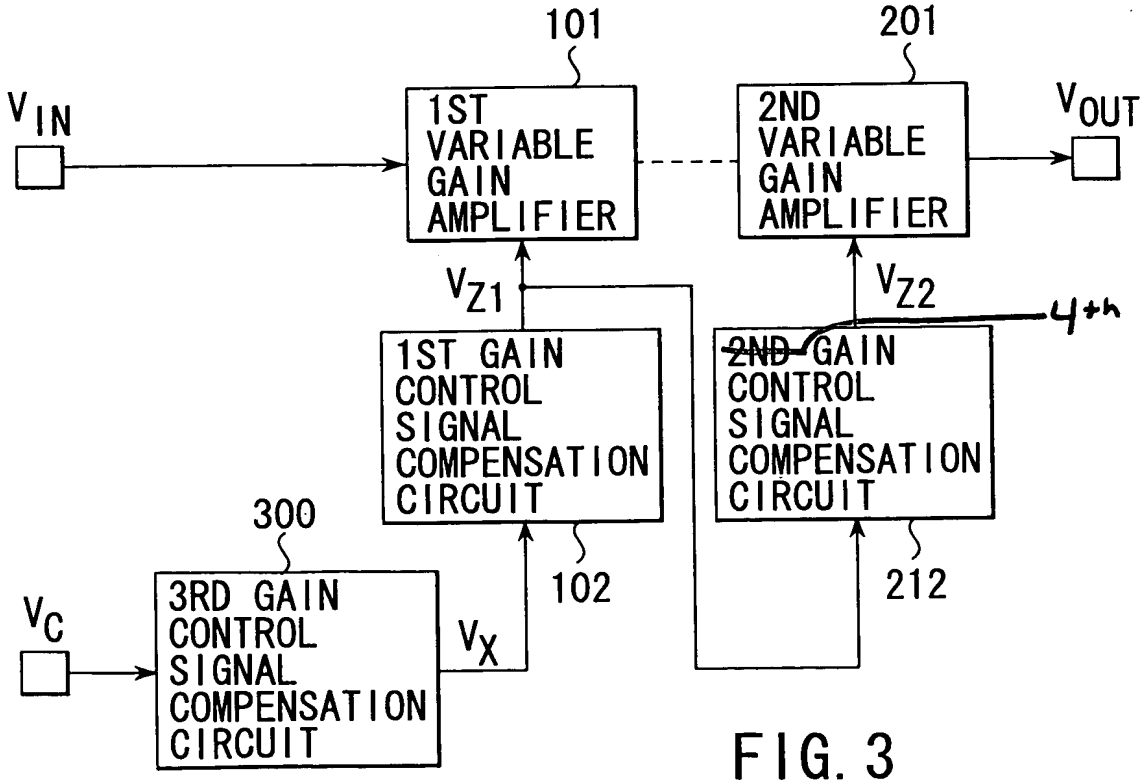

FIG. 3

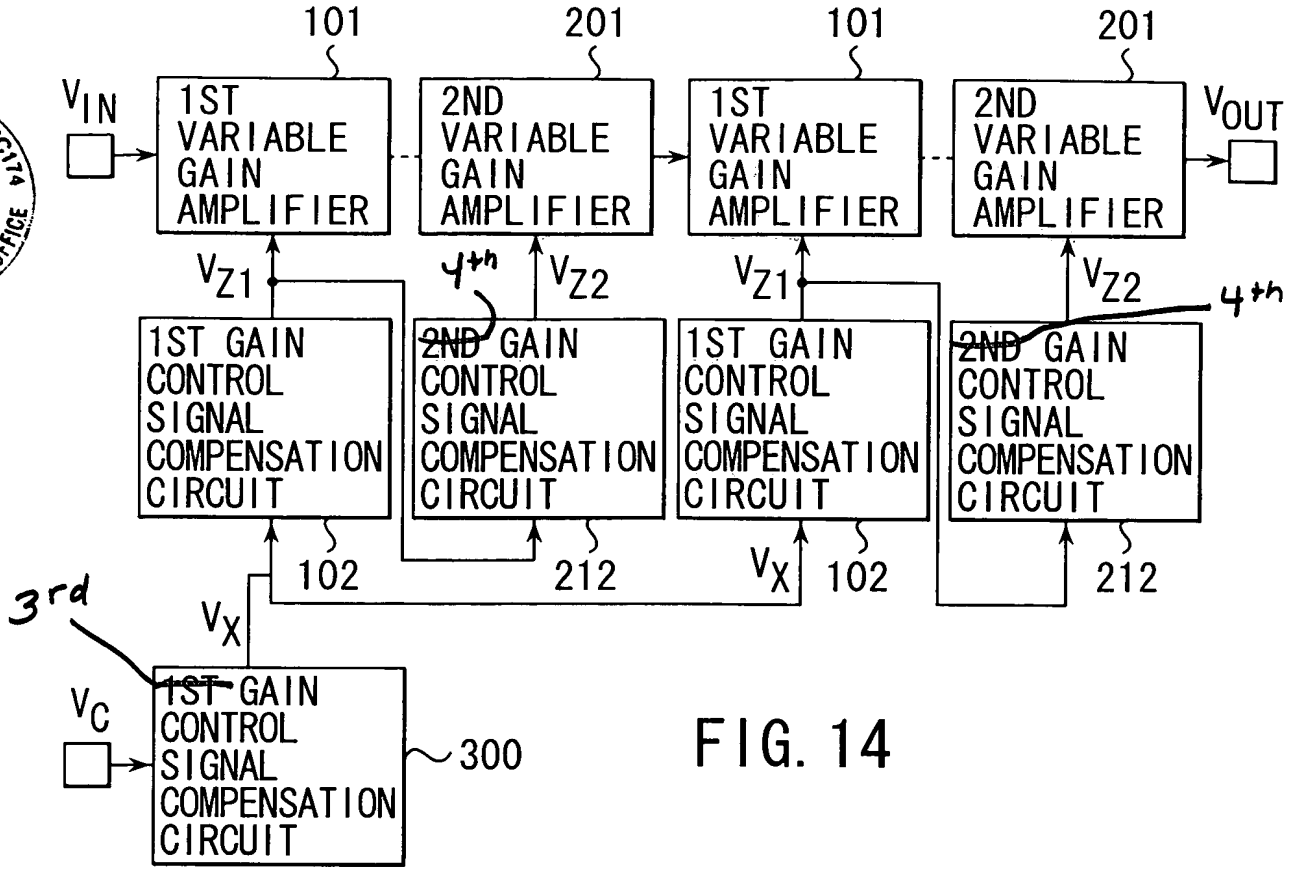

FIG. 14

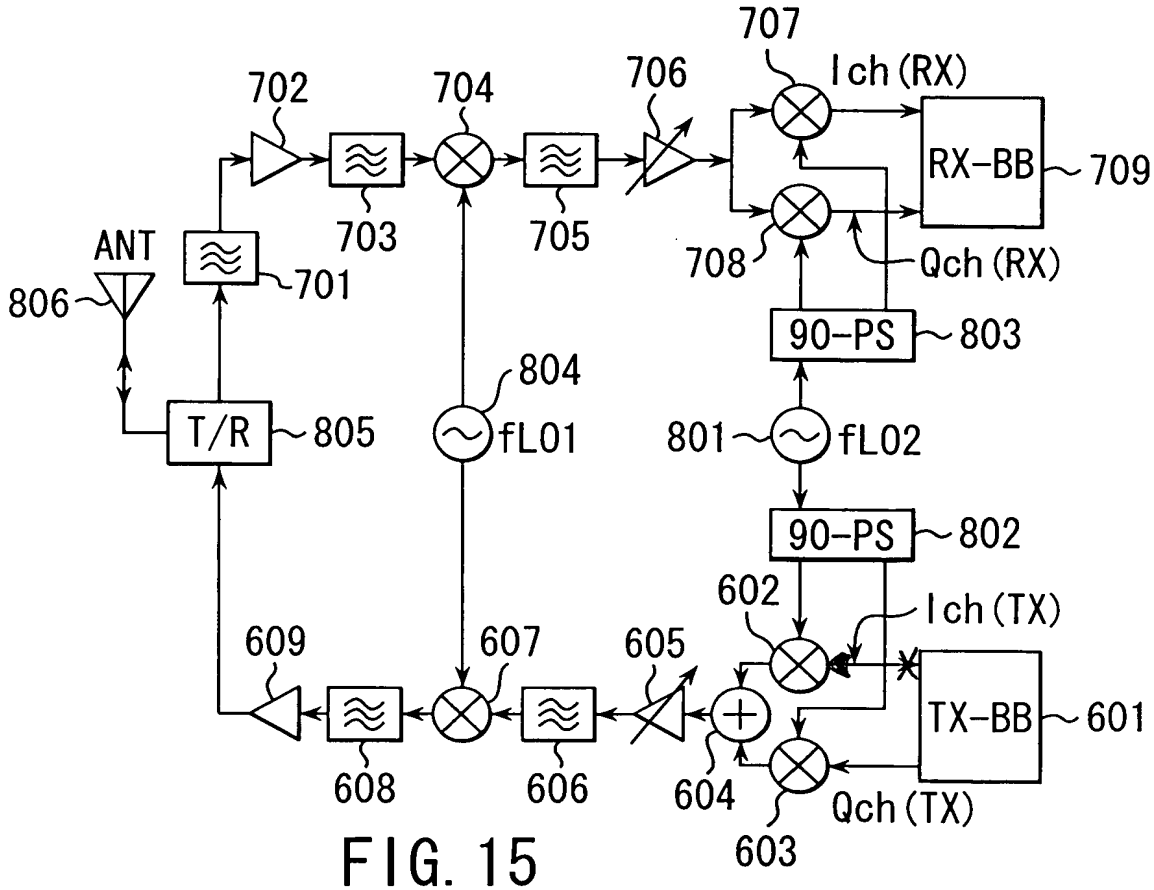

FIG. 15

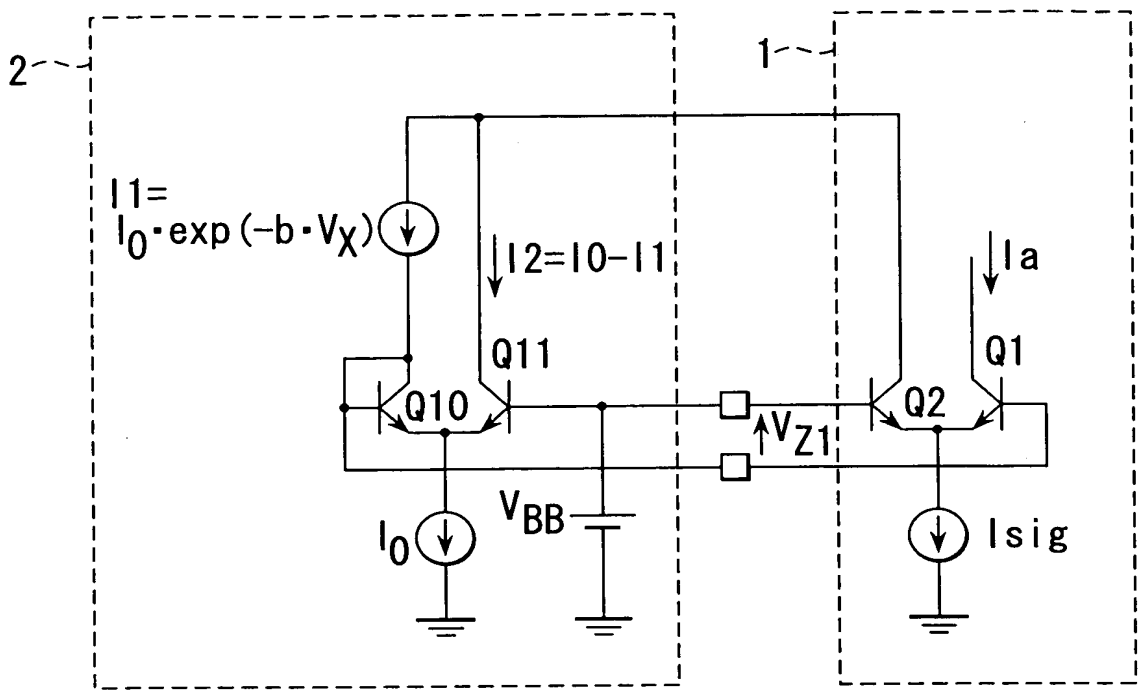

FIG. 16
(PRIOR ART)

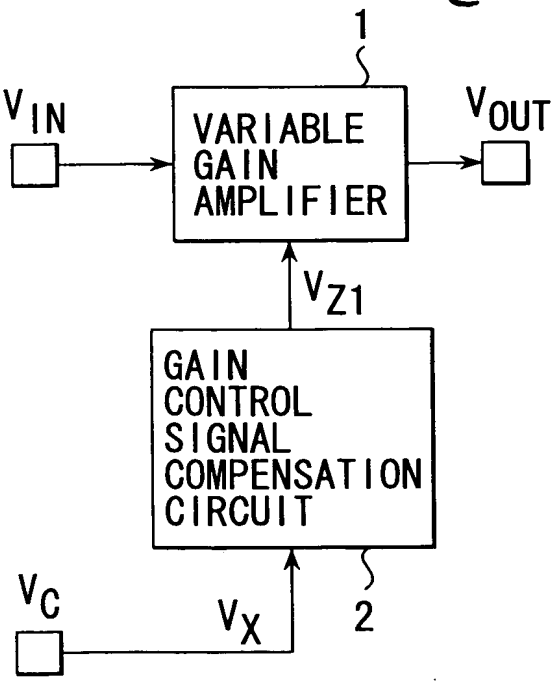

FIG. 17A
(PRIOR ART)

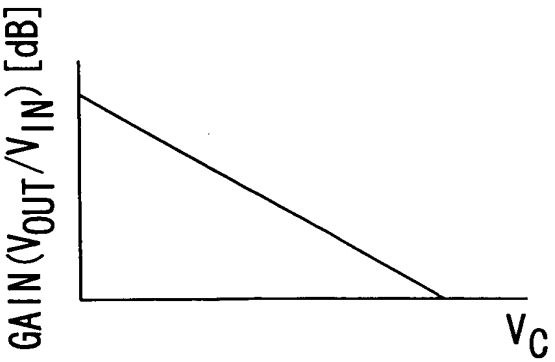

FIG. 17B

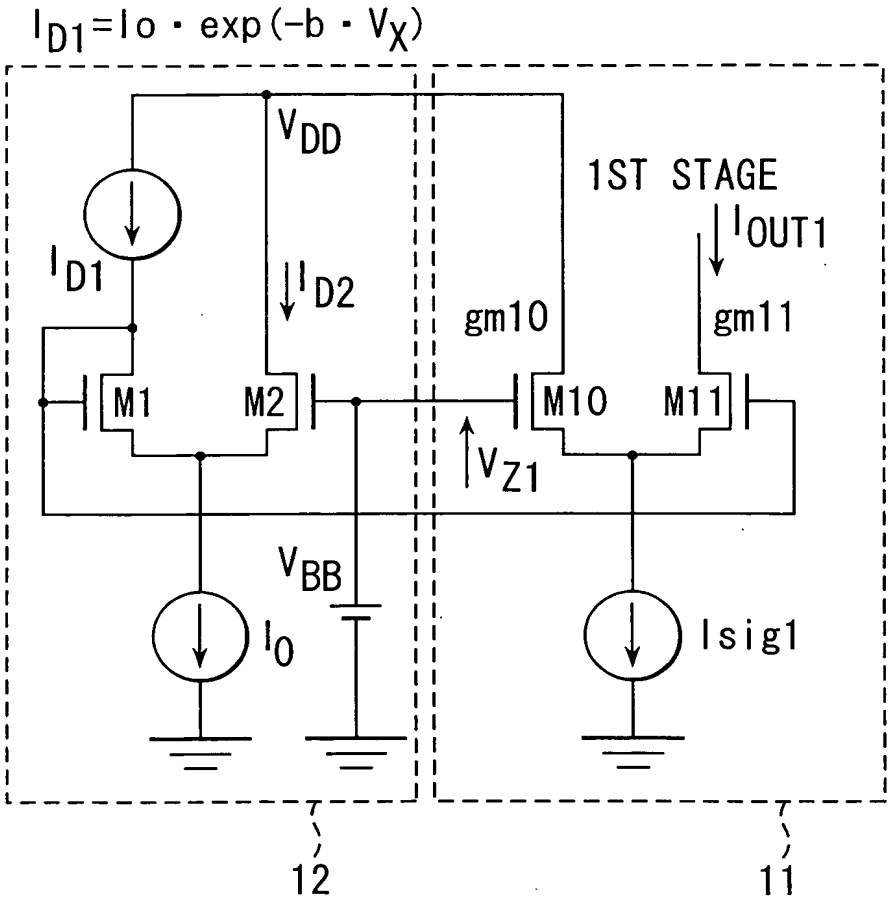

FIG. 18
(PRIOR ART)